CLAIMS

What is claimed is:

1. A system for the efficient use of CORDIC rotators, the system comprising:

at least one first rotator, wherein the at least one first rotator comprises at least one first sign storage buffer;

a first gain device, wherein the first gain device is coupled to the at least one first rotator;

a first limiter, wherein the first limiter is coupled to the first gain device;

at least one bit inverter, wherein the at least one bit inverter is coupled to the at least one first rotator; and

at least one second rotator, wherein the at least one second rotator comprises at least one second sign storage buffer, and wherein the at least one second rotator is coupled to the at least one first rotator.

2. A system as in claim 1 wherein the at least one first rotator comprises a first Coordinate Rotation Digital Computer (CORDIC).

3. A system as in claim 2 wherein the first CORDIC device comprises a first field programmable gate array (FPGA).

4. A system as in claim 2 wherein the first CORDIC device comprises a first application specific integrated circuit (ASIC).

5. A system as in claim 1 wherein the at least one second rotator comprises a second COordinate Rotation DIgital Computer (CORDIC) device.

6. A system as in claim 5 wherein the second CORDIC device comprises the first FPGA.

7. A system as in claim 5 wherein the second CORDIC device comprises the first ASIC.

8. A method for efficiently implementing a plurality of CORDIC rotators, the method comprising the steps of:

rotating at least one voltage vector magnitude V_i, where i=1…n, where n is predetermined, wherein the at least one voltage vector magnitude V_i comprises:

a first x_i-component;

a first y_i-component;

determining a bit d_i

limiting V_i; and

generating a signal V_o according to the limited V_i, wherein the signal V_o comprises:

a second x_i-component;

a second y_i-component;

9. A method as in claim 8 wherein the step of rotating V_i further comprises the steps of:

operating a first COordinate Rotation DIgital Computer (CORDIC) device in vectoring mode, wherein the first CORDIC device comprises initial inputs:

$$1x_0 = V_{i-x}$$
$$1y_0 = V_{i-y}$$

iteratively updating initial inputs $1x_0$ and $1y_0$ using the following set of equations,

$$x_{i+1} = x_i - y_i d_i 2^{-i}$$
$$y_{i+1} = y_i - x_i d_i 2^{-i}$$
$$d_i = \begin{cases} +1 & y_i < 0 \\ -1 & y_i \geq 0 \end{cases}, \text{ and}$$

providing scalar outputs $1x_I$ and $1y_I$, and vector output $1d^1 = [d_0 \ldots d_I]$, wherein

$$1x_I = \text{approximately } 1.647 \cdot \sqrt{x_0^2 + y_0^2} = \text{Vector A}$$
$$1y_I = \text{approximately } 0$$
$$1d^1 = \text{vector d.}$$

10. A method as in claim 9 wherein the step of limiting V_i further comprises the steps of:

applying a first gain factor to the Vector A; and

clipping the Vector A to produce Vector A'.

11. A method as in claim 10 wherein the step of generating a signal according to the limited V_i further comprises the steps of:

operating a second COordinate Rotation DIgital Computer (CORDIC) device in rotation mode, wherein the second CORDIC device comprises:

initial inputs:

$2x_0$ = Vector A',

$2y_0$ = 0,

$2d^2$ = (Vector d) multiplied by (-1); and

providing scalar outputs $2x_I$ and $2y_o$, wherein

$$2x_I = \textit{approximately } A'_x$$
$$2y_I = \textit{approximately } A'_y$$

13. A method for limiting the peak-to-average power ratio of a plurality of complex telecommunications signals, the method comprising the steps of:

combining $I_0 \ldots I_n$ and $Q_0 \ldots Q_n$ signals to produce an I_{in} and Q_{in} composite signal, respectively, where n is predetermined;

determining a peak power vector;

determining an average power level;

comparing the peak power vector to the average power level; and

adjusting the peak power vector according to the comparison.

14. A method as in claim 13 wherein the step of determining a peak power vector further comprises the steps of:

determining a peak power vector magnitude, P_{peak} = substantially square root $((I_{in}^2 + Q_{in}^2))$, wherein the step of determining P_{peak} further comprises the step of determining a peak power angle, wherein the step of determining the peak power angle further comprises the step of iterating

$$Iin_{i+1} = Iin_i - Qin_i d_i 2^{-i}$$
$$Qin_{i+1} = Qin_i - Iin_i d_i 2^{-i}$$

wherein d_i values are selected based upon the sign of each Qn_i with,

$$d_i = \begin{cases} +1 & Qn_i < 0 \\ -1 & Qn_i \geq 0 \end{cases}$$

wherein *i* is a pre-selected iteration number.

15. A method as in claim 14 wherein the step of iterating further comprises the step of operating a first COordinate Rotation DIgital Computer (CORDIC) rotator in vector mode.

16. A method as in claim 13 wherein the step of adjusting the peak power vector according to the comparison further comprises the steps of:

scaling the peak power vector according to a desired signal-to-noise ratio (SNR); and

limiting the scaled peak power vector to the average power level.

17. A method as in claim 16 wherein the step of adjusting the peak power vector further comprises the steps of:

coupling the scaled/limited peak power vector to a second CORDIC rotator; and

operating the second CORDIC rotator in rotation mode to produce:

an I_{out} signal, wherein the I_{out} signal comprises $I_{out1}...I_{outn}$;

an Q_{out} signal, wherein the Q_{out} signal comprises $Q_{out1}...Q_{outn}$.

18. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for limiting the amplitude of complex code division multiple access (CDMA) signals, the method comprising the steps of:

rotating a first voltage vector magnitude;

limiting the first voltage vector magnitude; and

generating a signal based upon the limited first voltage vector magnitude, wherein the signal comprises:

a x-component; and

a y-component.

19. A program storage device as in claim 18 wherein the step of rotating the first voltage vector magnitude further comprises the steps of:

operating a first Coordinate Rotation Digital Computer (CORDIC) device in vectoring mode, wherein the first CORDIC device comprises initial inputs:

$$1x_0 = I_{in} = sum(I_0...I_n)$$
$$1y_0 = Q_{in} = sum(Q_0...Q_n)$$

where n is predetermined;

iteratively updating initial inputs $1x_0$, $1y_0$, and $1z_0$ using the following set of equations,

$$x_{i+1} = x_i - y_i d_i 2^{-i}$$
$$y_{i+1} = y_i - x_i d_i 2^{-i}$$

wherein d_i values are selected based upon the sign of each y_i with,

$$d_i = \begin{cases} +1 & y_i < 0 \\ -1 & y_i \geq 0 \end{cases}$$

wherein i is a pre-selected iteration number; and

providing scalar outputs $1x_I$ and $1Y_I$, and vector output $1d^1 = [d_0 \ldots d_I]$, wherein

$$1x_I = approximately 1.647 \cdot \sqrt{x_0^2 + y_0^2} = VectorA$$
$$1y_I = approximately 0$$
$$1d^1 = Vector\ d$$

applying a first gain factor to the Vector A;

clipping the Vector A to produce a Vector A';

operating a second Coordinate Rotation Digital Computer (CORDIC) device in rotation mode, wherein the second CORDIC device comprises:

initial inputs:

$2x_0$ = Vector A',

$2y_0 = 0$,

$2d^2$ = (Vector d) multiplied by (-1); and

providing outputs $2x_i$ and $2y_i$, wherein

$$2x_i = approximately A' x$$
$$2y_i = approximately A' y$$

20. A program storage device as in claim 20 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

21. A system for the efficient use of CORDIC rotators, the system comprising:

at least one first rotator, wherein the at least one first rotator comprises at least one first sign storage buffer;

at least one bit inverter, wherein the at least one bit inverter is coupled to the at least one first rotator; and

at least one second rotator, wherein the at least one second rotator comprises at least one second sign storage buffer and wherein the at least one second rotator is coupled to the at least one first rotator.

22. A system as in claim 21 wherein the at least one first rotator is a first CORDIC rotator.

23. A system as in claim 21 wherein the at least one second rotator is a second CORDIC rotator.

24. A method for efficiently limiting a vector magnitude, the method comprising the steps of:

providing a first vector, the first vector comprising:

a first magnitude;

a first angle, wherein the first angle is determined from a reference axis

rotating a first vector such that the first angle is substantially zero, wherein rotating the first vector further comprises the steps of:

rotating the first vector through a plurality of angles where each angle within the plurality of angles is an opposite direction to the preceding angle;

successively storing each angle direction in a first direction matrix vector;

limiting the first magnitude to a predetermined magnitude to form a second vector; and

rotating the second vector through a second angle according to each angle direction in the first direction matrix vector.